AMENDMENTS TO THE CLAIMS

Please cancel claim 7 without prejudice.

1. (CURRENTLY AMENDED) A time-slot interchanger for interchanging the order of subframes of data within an input data frame comprising:

a global frame clock;

an interchange random access memory receiving the input data frame, out of alignment with the global frame clock, at an input;

a write address generator which addresses the interchange random access memory to write subframes, out of alignment with the global frame clock, in a received order, wherein the write address generator generates the write address from a count of a local frame counter synchronized to the input data frame; and

a read address generator which addresses the interchange random access memory to read subframes in interchanged order and aligned to the global frame clock, wherein the read address generator transforms a count of a global frame counter to generate the read address, the interchange random access memory comprises three buffers and the local frame counter includes a modulo 3 counter field which selects one of the three buffers.

2. (CANCELED)

3. (PREVIOUSLY PRESENTED) A time-slot interchanger as claimed in claim 1 wherein the global frame counter count is transformed in a random access memory.

4. (CANCELED)

5. (PREVIOUSLY PRESENTED) A time-slot interchanger as claimed in claim 1 wherein the interchange random access memory forms N > 2 buffers, the local frame counter being between one and N - 1 buffer lengths ahead of the global frame counter.

6. (ORIGINAL) A time-slot interchanger as claimed in claim 5 wherein the input data frames are SONET frames and the buffer length is a column length.

7. (CANCELED)

8. (ORIGINAL) A time-slot interchanger as claimed in claim 1 wherein the interchange random access memory is noncontiguously addressed.

9. (PREVIOUSLY PRESENTED) A time-slot interchanger as claimed in claim 8 further comprising a predecoder which maps the noncontiguous address space to instantiated locations in the interchange random access memory.

10. (ORIGINAL) A time-slot interchanger as claimed in claim 9 wherein the predecoder includes at least one n-to-(2^n-p) decoder for some integers n and p.

11. (CURRENTLY AMENDED) A time-slot interchanger as claimed in claim 1 wherein the input data frames are SONET STS-M frames and each of the buffers in the interchange random access memory ~~includes three buffers, each of~~ comprise M bytes.

12. (ORIGINAL) A time-slot interchanger as claimed in claim 11 where M equals 48.

13. (ORIGINAL) A digital cross connect comprising plural switching stages, each stage having plural switches receiving plural frames of time multiplexed input data and switching the data in time and space, at least one switch of at least one stage comprising a time-slot interchanger as claimed in claim 1.

14. (PREVIOUSLY PRESENTED) A method of interchanging the order of subframes of data within an input data frame comprising:

providing a global frame clock;

at an input to an interchange random access memory, receiving the input data frames, out of alignment with the global frame clock;

generating write addresses which address the random access memory to write subframes, out of alignment with the global

frame clock, in a received order, wherein the write address is generated from a local frame counter synchronized to the input data frame; and

generating read addresses which address the random access memory to read subframes in interchanged order and aligned to the global frame clock, wherein the interchange random access memory comprises three buffers and the local frame counter includes a modulo 3 counter field which selects one of the three buffers.

15. (ORIGINAL) A method as claimed in claim 14 wherein the read address is generated by transforming a global frame counter to generate the read address.

16. (ORIGINAL) A method as claimed in claim 15 wherein the global frame counter count is transformed in a random access memory.

17. (CANCELED)

18. (PREVIOUSLY PRESENTED) A method as claimed in claim 14 wherein the interchange random access memory forms $N > 2$ buffers, the local frame counter being between one and N-1 buffer lengths ahead of the global frame counter.

19. (ORIGINAL) A method as claimed in claim 18 wherein the input data frames are SONET frames and the buffer length is a column length.

20. (CANCELED)

21. (PREVIOUSLY PRESENTED) A method as claimed in claim 14 wherein the interchange random access memory is noncontiguously addressed.

22. (ORIGINAL) A method as claimed in claim 21 further comprising predecoding addresses to the random access memory to map the address space to instantiated locations in the random access memory.

23. (PREVIOUSLY PRESENTED) A method as claimed in claim 22 wherein predecoding addresses to the random access memory is performed using at least one n-to-(2^n-p) decoder for some integers n and p.

24. (ORIGINAL) A method as claimed in claim 14 wherein the input data frames are SONET STS-M frames and the interchange random access memory includes three buffers, each of M bytes.

25. (ORIGINAL) A method as claimed in claim 24 where M equals 48.

26. (ORIGINAL) A method as claimed in claim 14 further comprising, in plural switching stages, receiving plural frames of time multiplexed input data and switching the data in time and space, the order of subframes being interchanged as recited in claim 13.

27. (PREVIOUSLY PRESENTED) A time slot interchanger for interchanging the order of subframes of data within an input data frame comprising:

a global frame clock;

interchange random access memory means for receiving the input data frame, out of alignment with the global frame clock;

write address generator means for addressing the interchange random access memory means to write subframes, out of alignment with the global frame clock, in a received order; and

read address generator means for addressing the interchange random access memory means to read subframes in interchanged order and aligned to the global frame clock, wherein the interchange random access memory includes three buffers and the write address generator means includes a modulo 3 counter field which selects one of the three buffers.

28. (PREVIOUSLY PRESENTED) A time-slot interchanger as claimed in claim 1 further comprising a multiplexer circuit configured to generate said global frame clock by multiplexing an external frame clock input and a plurality of start of frame

signals, wherein each of the start of frame signals is synchronized to a respective one of a plurality of data inputs.

29. (CURRENTLY AMENDED) A time-slot interchanger ~~as claimed in claim 1 wherein~~ for interchanging the order of subframes of data within an input data frame comprising:

a global frame clock;

an interchange random access memory receiving the input data frame, out of alignment with the global frame clock, at an input;

a write address generator which addresses the interchange random access memory to write subframes, out of alignment with the global frame clock, in a received order, wherein the write address generator generates the write address from a count of a local frame counter synchronized to the input data frame; and

a read address generator which addresses the interchange random access memory to read subframes in interchanged order and aligned to the global frame clock, wherein (a) the read address generator transforms a count of a global frame counter to generate the read address and (b) the global frame counter comprises~~:~~ (i) a delay block configured to receive the global frame clock and present a start of frame signal, wherein the delay block delays the frame clock by a predetermined number of byte clocks~~;~~, (ii) a first divider configured to generate a subframe field of the global frame counter count in response to the start of frame signal and the byte clock~~;~~, (iii) a second divider configured to generate a column

field of the global frame counter count in response to the start of frame signal, the byte clock and an output of the first divider, (iv) a third divider configured to generate a column-group field of the global frame counter count in response to the start of frame signal, the byte clock and an output of the second divider, and (v) a fourth divider configured to generate a row field of the global frame counter count in response to the start of frame signal, the byte clock and an output of the third divider.